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# Universal Synthesizer for Frequencies up to and above 1000 MHz Part 1

**The following article describes a frequency synthesizer circuit whose hardware must be complimented by appropriate software in order that it can be conditioned to fulfil a variety of functions. The highest frequency, for the time being, is about 1 GHz but the further development of the pre-scaler section can lead to the extension of this limit to higher realms. Owing to the employment of the most modern integrated technology, the performance can be achieved with the minimum of power consumption thus making it very suitable for portable work. Besides the digital portion, two differing oscillator circuits will be considered which are optimised for the frequency in use.**

## 1. CIRCUIT CONCEPT

### 1.1. General

The basic idea of a PLL synthesizer oscillator is to produce a multitude of frequencies with a defined frequency separation by means of a main oscillator and a reference oscillator, utilising digital techniques to achieve this aim. The theoretical advantage with this method is that no mixer or filters are necessary in the signal path and therefore the production of undesired spurious mixing products is avoided.

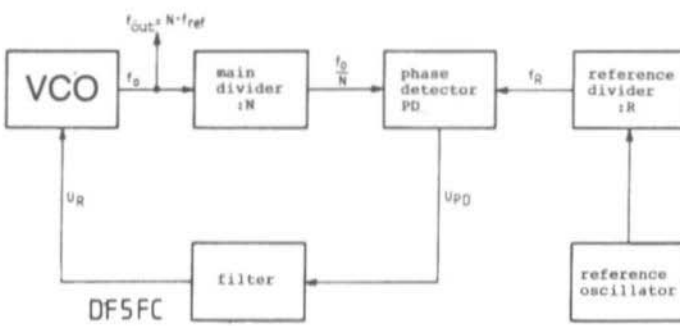


**Fig. 1: Basic block schematic of a PLL synthesizer**

The output frequency of the Voltage Controlled Oscillator (VCO) is brought to the reference frequency $f_r$ via a programmable divider N as shown in **fig. 1**. This reference frequency represents the frequency separation of all juxtaposition signals which form the output "comb" of frequencies – or channels. The divider R divides down the output frequency of a crystal-controlled reference oscillator to the value of that possessed by the separation (step) frequency – this is again, the reference frequency $f_{ref}$. The crystal oscillator determines the frequency stability of all the frequencies available in the output. The two derived frequencies are then compared in a frequency and phase detector. This delivers an output pulse train which varies in accordance to which of the two comparison frequencies is the highest. This pulse train is then filtered and the integrated output, which forms the tuning voltage, then controls the VCO. The circuit thereby causes the two inputs to the phase detector to lock together and maintains them in this condition by correcting the VCO as required. When now, the divider N is required to shift to a one higher increment in frequency, the frequency at the PD at that instant, is lower than that demanded. The VCO frequency is then raised until the original conditions of frequency balance are achieved. The output frequency then moves up to the new channel. The whole process is effectively the same, but reversed, when the value of N is required to be smaller.

The technical limits of this process are set by the programmable divider. Because of their internal transit times, they have a relatively low, higher frequency limit. With ECL chips, this limit lies around 60 to 80 MHz and with modern C-MOS ICs, 15 to 20 MHz can be achieved. The direct use of any ICs for this purpose is not possible at 145 MHz. The limit for highly integrated dividers in both MOS or in TTL is not very much higher. For all higher frequency applications the VCO frequency must be brought down to the frequency of the programmable divider. There are three techniques for doing this:

- Mixing
- PLL with a fixed pre-scaler
- PLL with a switchable pre-scaler (swallow or modulus divider)

The first two techniques will now be considered briefly together with their relative advantages and disadvantages. The third will be described in some detail.

### 1.2. The Mixing Synthesizer

The block diagram of **fig. 2** differs from fig. 1 owing to the addition of a mixer and a local oscillator. The local oscillator works at a frequency which is 5 to 10 MHz lower than the VCO, depending on the type of divider in use. It is crystal controlled and could also contain a multiplier.

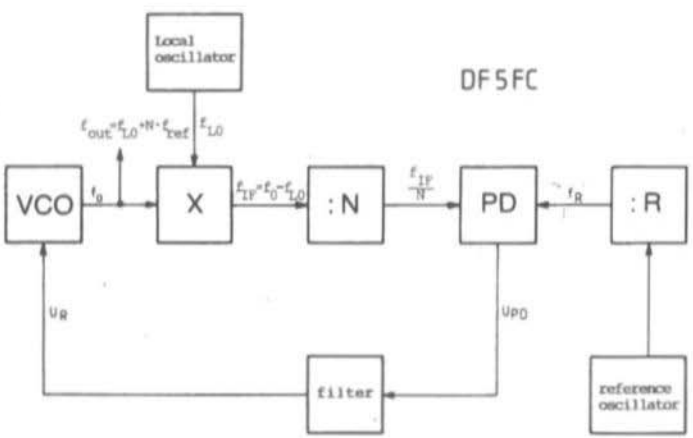


**Fig. 2: Synthesizer with mixer and local oscillator**

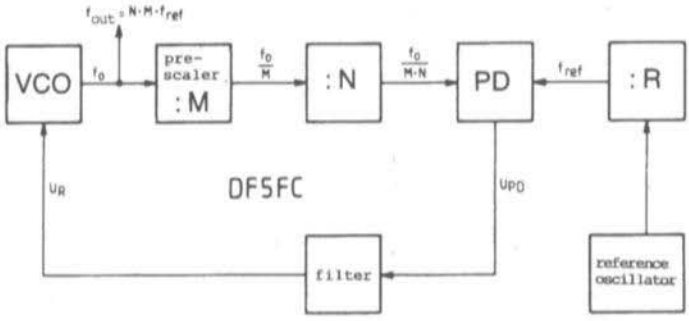


**Fig. 3: Synthesizer with a fixed pre-scaler**

The advantage of this circuit is that, despite a small step frequency, a signal with a relatively low phase-noise can be obtained. This, of course, presumes that all oscillators are constructed in accordance with good practice and that the rest of the circuit is very carefully dimensioned. Furthermore, a quasi-continuous tuning can be realised, if the local oscillator can also be tuned over a small range. A large proportion of modern radio equipment, having continuous tuning, works using this principle. It does require a certain complexity in the tuning circuits but this presents no difficulties for modern microprocessors.

The disadvantage of this circuit is the complexity of the circuitry which is required. Looking at circuits which were published some time ago in VHF COMMUNICATIONS, for example "Südwind" by DJ8IL in (1) or the 2-metre synthesizer by DC1QW in (2), it can be seen that as well as the actual digital part, which did not need alignment, the local oscillator multiplier and mixer stages all were present. This sort of circuit technique is always prone to the risk of spurious outputs and false locking of the PLL.

The use of the mixer limits the tuning range of the circuit. Theoretically, band segments are received whose range extends from zero Herz up to the maximum working frequency of the dividers. When a broadband equipment is required, several down-conversions (with their oscillators) are necessary. Another problem occurs when the local oscillator is brought too near the working frequency inasmuch that the PLL locks to the image frequency.

This would mean that for a universal synthesizer, a different mixer crystal must be employed for each application. This also entails a different dimensioning of the multiplier for each case. This is a much too high a price to pay in terms of complexity and on these grounds the technique was not considered further. Another disadvantage is that the LO is normally very close to the output frequency. If the whole unit is not very carefully constructed, a large component of the oscillator power appears in the output. Filtering out the unwanted LO power is difficult owing to the close proximity of the wanted signal.

### 1.3. Synthesizer with Fixed Pre-Scaler

This circuit obviates the use of local oscillators as the diagram of **fig. 3** shows. The circuit complexity remains within bounds and the actual circuit has no alignment stages to bother with. The overwhelming disadvantage lies in the use of the fixed pre-scaler. The inherent problem is that the size of the incremental steps cannot be constant as they are determined by N * M where M is the dividing factor of the pre-scaler. In order to obtain the required constant steps in frequency, the reference frequency must also be divided by M in sympathy. But this means that the reference frequency must drop which has a deleterious effect upon the phase loop (see filter calculation in appendix). Owing to the low reference frequency, the loop filter must also be designed for a low limit frequency which entails a lengthening of the time required for the lock to occur. This is unacceptably long when, in operation, large frequency spans are switched and the control

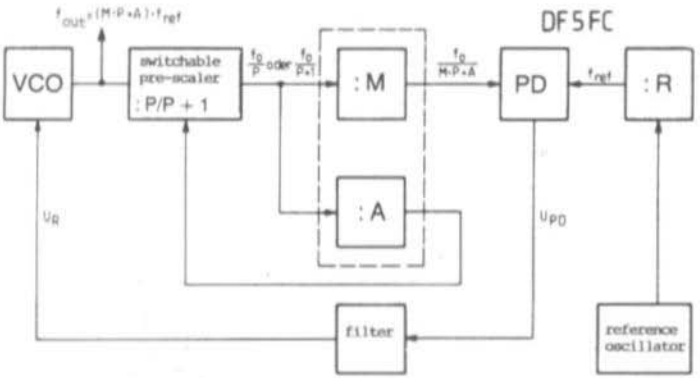


**Fig. 4: Synthesizer with a dual-modulus pre-scaler**

voltage is hunting towards the selected frequency. It is tolerable only for fixed channel equipment.

A low-frequency loop filter also tends to inhibit the property of the loop to phase out spurious signals. Also, the reference frequency tends to appear in the loop control voltage which causes a spectral comb of frequencies to occur in the output of the VCO. This problem is, of course, inherent in all synthesizers but it is exacerbated when the loop frequency is low. Circuits of this type have been described by Helpert (3) in his "Gartenzwerge" transceiver article.

This form of circuit is very suitable when the required step frequency is to be very large as, for example, in a converter local oscillator. In a 23 cm transverter, the local oscillator could have frequency incremental steps of 2 MHz. This would entail a reference frequency of 31.25 kHz – even if a divider scaling factor of 64 is used. The technique is also suitable for employment as a local oscillator for a down-converter synthesizer, but the frequency planning must be given due consideration (4). The output signal contains no spurs as only one oscillator is working. It is not suitable, however, for the planned universal synthesizer as the reference frequency must sink to an unacceptably low value.

### 1.4. Synthesizer with a Variable Pre-Scaler (Dual Modulus Divider)

In this type of circuit (**fig. 4**), a pre-scaler having a variable divider precedes the "N"-divider. The division factor can be switched over by a control logic from a programmable divider. This has the effect that the intended step increments are obtained despite the pre-scaling and without changing the reference frequency. The loop is easier to arrange and does not carry the disad-

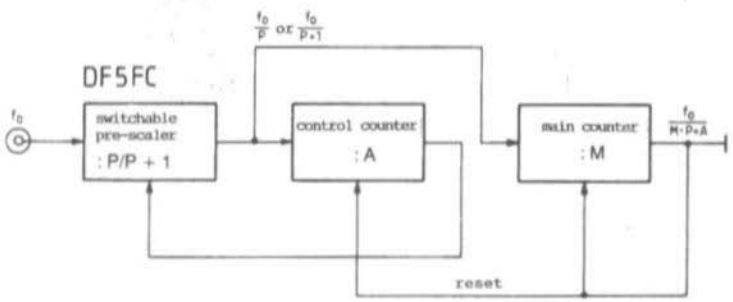


**Fig. 5: Principle of dual-modulus pre-scaler**

vantages of a fixed pre-scaler. Simply programming the main divider allows a very large frequency range to be spanned, making this circuit variant seems a suitable candidate for the universal synthesizer. Because of the absence of an LO/mixer there are no tuning points. Continuous tuning, within certain limits, is possible by making the reference frequency tunable.

At first sight, this type of frequency processing seems rather complicate. If the complete divider block is closely examined and the sequences taken separately, there is nothing terribly difficult about it. The diagram of **fig. 5** will help to explain its function.

The following conditions are assumed to begin the functional explanation:

1. The pre-scaler divides by factors of P and P + 1, switchable via the modulus control.
2. The dividers A and M are down-wards counters which, together with a reset pulse, are set to the pre-determined value, both of which are **not allowed** to underflow zero.
3. The A-counter is **always** set to a smaller number than the M-counter which means that is **always** the first one to reach zero.

It is assumed that both counters have just been set to their pre-determined value and that the counting cycle has started afresh. It is now necessary to consider how many VCO oscillations are necessary in order to obtain this condition again. This number will then correspond to the scaling factor of the circuit.

To start with, the pre-scaler is switched to P + 1. Since the A and the M counters have been switched in parallel, each time after P + 1 oscillations of the VCO by an impulse from the pre-scaler, the counter condition is stepped one lower. If, for example, the A counter has been set to 7, it has reached zero after 7 * (P + 1) (or in general after A * (P + 1) oscillations, with A as the pre-determined value. Because they are connected in parallel, the M counter has also decreased by a count of 7 (or in general, by A), its actual value is now M-7 (M-A). The A counter, upon reaching zero, initiates a signal which switches the pre-scaler over from P + 1 to P. The A counter locks itself so that it now works only in conjunction with the M counter. Now, each time after P oscillations of the VCO it is decreased by 1 until it also reaches zero i.e. (M-A) * P. The output of the counter controls, on the one hand, the phase discriminator, and, on the other hand, the reset logic. Upon the M counter reaching the count of zero, both counters are reset back to their original condition and the whole cycle starts all over again.

The total number of oscillations which were undertaken by the VCO in order to run through this sequence of events, is a consequence of the sum of the A counter A * (P + 1) and the **remainder** sum of the M counter (M-A) * P, that means:

$$\begin{aligned} N_{tot.} &= A\,(P + 1) + (M\text{-}A) * P \\ &= A * P + A + M * P - A * P \\ &= A + M * P \end{aligned} \qquad (1)$$

In order to clarify this, an actual numerical example is considered.

P = 40, i.e. P + 1 = 41, (determined by the type of pre-scaler).

The M counter is pre-adjusted to the figure 362 (M = 362).

The A counter is pre-adjusted to the figure 20, (A = 20).

This means: that the VCO signal is divided 20 times by a factor of 41 and then 342 times (M-A) by 40. This results in a total divisor of:

$$N_{tot.} = 20 + 40 * 362 = 14500$$

This count is appropriate to a 2 metre transmitter which is tunable in 10 kHz increments:

$$N_{tot.} * f_{ref.} = f_{VCO}$$

When considering this procedure, the following limitations must be mentioned. The most important one is that imposed by the pre-scaler. This has a lower limit, beneath which, frequencies are completely unobtainable. If the formula of (1) is resolved, the result will be obtained for when P = 40 (typical value for these pre-scalers):

$$N = 40 * M + A$$

Now it may be imagined that M is a decade value (better, a multiplier by 40) and A is in units (A runs from 0 to 39). Under the conditions initially mentioned, that M must always be greater than A,

results in the fact that M must also be at least equal to 40. When M is smaller, the reset condition is attained (counter A and M are connected in parallel, see fig. 5), before P + 1 is switched over to P. In this manner, the units presented by the A counter are never reached and the process goes no further. The minimum divisor of M must therefore be:

$N_{min.} = 40 * 40 = 1600$ or in general $N_{min.} = (P)^2$ (2)

This condition is important if the pre-scaler has a large P, because high frequencies must then be processed. The Plessey NJ8820 used here (to be considered later in more detail) has a specified worst-case working frequency of 10.6 MHz. This value should not be exceeded bacause it causes interference to the internal pulse sequencing (the internal gate transit-times limit the scaling, depending upon the adjusted numerical value of the divisor). This results in frequencies being generated other than those which have been pre-determined (e.g. some channels more or less). For a 1.3 GHz VCO a pre-scaler with a divisor of, for example 128/129 should be chosen. The maximum input frequency to the PLL chip is then approximately 10.2 MHz which is just about admissible. The minimum divisor is therefore:

$$N_{min.} = (128)^2 = 16384$$

For a required frequency incremental step of say 10 kHz the lower limit would be: 16384 * 10 kHz = 163.84 MHz. This arrangement would not be very suitable for a 2-metre radio. A further limitation is occasioned by the PLL chip itself. The maximum value for M is here 1023 and for A is 127 (for NJ8820). The dividing process treated here would result in the evaluation of the division factor for a frequency in the following manner:

Maximum working frequency/step = $N_{max.}$ (3)

Value for M counter: $M = N_{max.}/P$ (4)

From this result the whole number before the comma is directed to the M counter. The value after the comma is again multiplied by P, the resulting whole figure is the value for the A counter.

For example:
Maximum working frequency, 1300 MHz
Channel step, 10 kHz:

1300 MHz/10 kHz = 130000 = $N_{max.}$

M = 130000/128 = 1015.625
M = 1015

A = 0.625 * 128 = 80

This example makes it clear that the limit for M is rather extended. If, using this calculation, the upper limit is reached, then another step must be chosen in order that $N_{max.}$ is reduced; e.g. 25 kHz – or another scaling factor may be required.

The disadvantage of this PLL technique is that modulation of the loop control-voltage with the switching frequency of the pre-scaler takes place. Because of the constantly changing pre-scaler divisor, the pulse-length at the input of the phase detector also changes. This superimposed frequency is very low making it difficult to be filtered out in the loop. It manifests itself as an audible rumble in SSB receivers. This indicates that this narrow-band concept for the synthesizer is only usable within certain limits. Owing to the use of the double phase-detector and by careful construction, this feed-through can be kept to low limits. In commercial practice (signal generators up to 1000 MHz from almost all well-known manufacturers), this effect is minimised by a judicious amount of a counter voltage. This is possible since the superimposed frequency is derived directly from the division factor and can therefore be used for compensation. Th required complexity is extensive and would be much too much for any home-brewed amateur equipment.

**To be continued**

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# Universal Synthesizer for Frequencies up to and above 1000 MHz Part 2 (Conclusion)

## 2. CIRCUIT DESCRIPTION

Integrated circuits for use in synthesizers are offered by a number of firms; the choice fell here upon an IC-family from Plessey. These chips contain the most interesting phase detectors (to be precise two – one digital and one analogue – which share the work), moreover, the synthesizer processor employed has the means to control an EPROM automatically in order to obtain all operational information there. The chip also contains the sequence control together with almost all the components belonging to a PLL circuit. It can be so connected, that in normal operation, no access to the PROM is carried out thereby minimising interference signals on the output caused by internal control signals. The pre-scalers are also from Plessey in order to eliminate the possibility of interface problems. There is deliberately no description of similar chips from this series with micro-processor control as the required control computer would restrict the circle of users. **Figure 6** shows the central part of the circuit with pre-scaler, PLL IC, EPROM and loop filter.

The RF signal from the oscillator is taken via a buffer amplifier with variable pre-scaler. The amplifier is not used here to increase the level (the IC is relatively sensitive), but should improve the isolation between the analogue and digital sections of the circuit. It is important that de-coupling arrangements are employed in the supply line in the interests of obtaining a clean output signal. Many tests have proved that the dual-gate MOSFET circuit has the highest isolation properties from output back to input. A BF981, or equivalent, is satisfactory up to about 200 MHZ but for higher frequencies the later types, such as the BF966 or the BF988, are particularly suitable. The divided signal is taken directly to the PLL IC. This contains, as already mentioned, all the other parts of the PLL. In this circuit, the built-in crystal oscillator is also used.

In order to reach frequencies which are located between two step frequencies, one varicap diode is connected across the crystal. For a simple manual tuning operation this circuit is sufficiently linear. The reference crystal is taken to be 4 MHz. According to the data sheet, frequencies up to 10 MHz are possible; the reference divider must then be programmed somewhat differently. The complete programme information is contained in

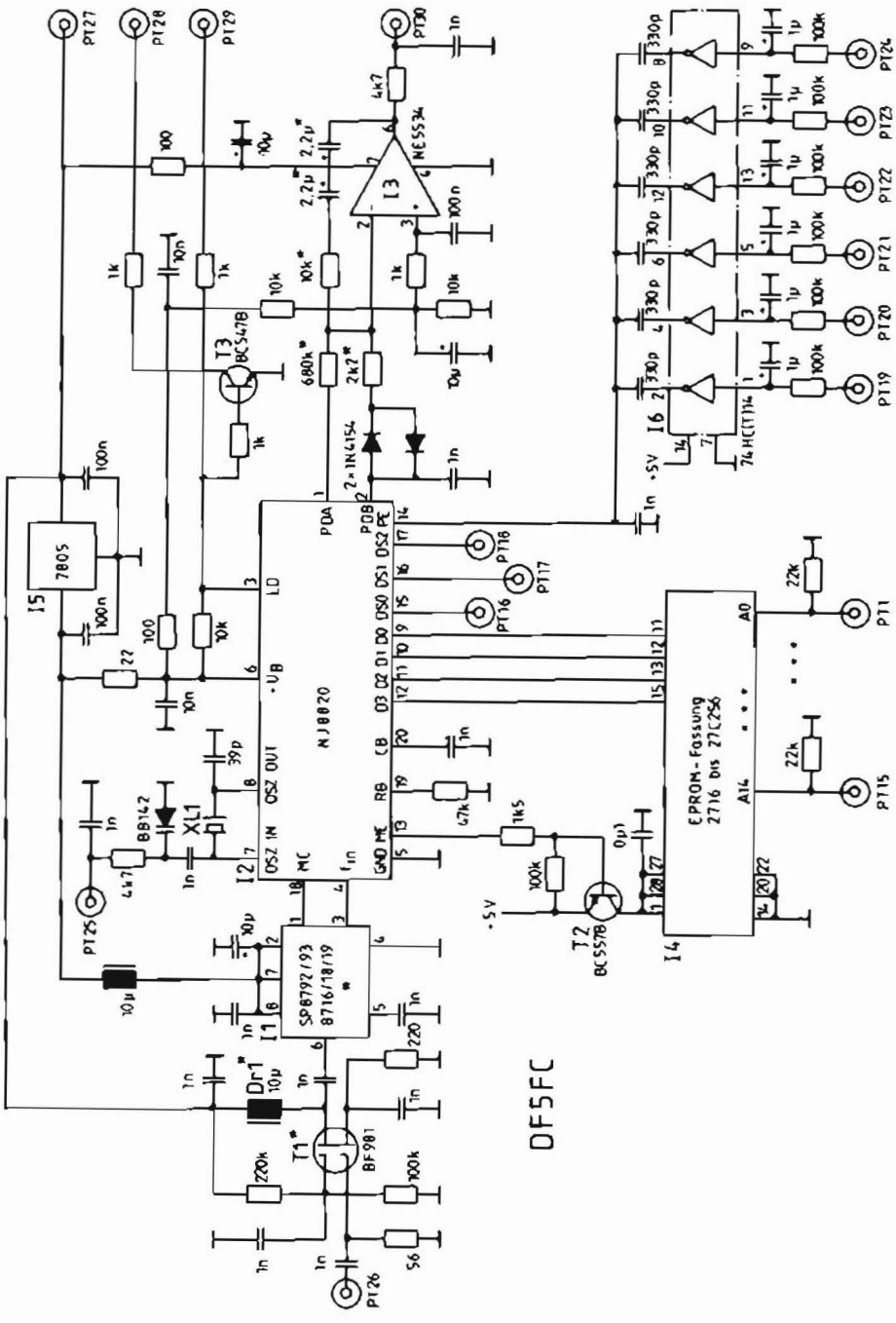


Fig. 6: Complete schematic of the synthesizer's PLL with the control E-PROM

an EPROM. It is so programmed that the receive frequency is selected directly at the switch. For send/receive switch-over, and for relay operation, further address lines can be used to change-over to the requisite set of data.

As mentioned previously, the IC contains two phase detectors. The digital phase detector is responsible for the control of large frequency differences, small deviations result in the sample-and-hold detector being engaged. This in its characteristic analogue PD has only a very small sample of the reference so that the spectral lines in the comb of frequencies are suppressed. Apart from that, it attenuates switching noises of all types from the digital section.

Both detectors in the IC are externally parallelled at their inputs, the auto switch-over is accomplished by the antiparallel connected diodes. If silicon diodes are employed for this purpose, the switch-over is carried out at a control-voltage surge of more than 0.7 V. The resistor RB and capacitor CB determine the loop gain of the sample-and-hold phase detector. The capture and control range of the phase detector and its response time are thereby determined. The values employed should be a good compromise for use in radio-equipment synthesizers. That is also, in general, applicable to loop filters.

As the oscillator trans-conductance always varies from one construction to another, there must be some attempt at matching for optimum operation. The first function is always possible with the dimensions as given. The annex contains some formulae with which calculations may be carried out. Further information can be found in the data-sheets/books (5) and (6) whereby the formulae in (6) are partially defective.

## 3. OSCILLATORS

### 3.1. Decoupling Arrangements

At this point, there must be some discussion about decoupling of the oscillator from the rest of the circuit, especially from the PLL chip, before going on to the actual oscillator description.

With a Voltage Controlled Oscillator (VCO), the tuning rate-of-response $K_{VCO}$ (Hz/V) must be kept firmly in mind. As an example, it will be supposed that the 70 cm band should be covered by both the transmitter and the receiver. Using an IF of 21.4 MHz, the final frequency minimum tuning range is 408.6 MHz to 440 MHz. This means a total range of altogether 31.4 MHz (highest transmit frequency 440 MHz to lowest receive frequency of 430 MHz minus the IF). At an available loop control voltage amplitude of 10 V (12 V minus the OP-amp. off-set voltage and an allowance for variations) result in a VCO sensitivity of 3.14 MHz/V. A loop-voltage variation of only 1 mV would result in a frequency change of 3.14 kHz! Loop voltage contamination of this order would result in an unusable input signal (FM noise modulation).

Included in these disturbing influences are variations in the supply voltage caused by mechanical vibrations (microphony) and changes in the load caused, for example, by internal changes to the switching divider which changes its resistance according to its input conditions. The supply-voltage fluctuations must be minimised with the aid of IC stabilizers. The self-generated noise of the latter must not be overlooked; see (7). The effect of load variations is avoided by using buffer stages at appropriate points. It is also helpful to reduce the coupling to the buffer stages to as low a value as possible. The resulting low loading also improves the quiescent stability of the circuit. The decoupling arrangements around the PLL IC are of the utmost importance.

### 3.2. FET Oscillator up to 200 MHz

In practice, two separate oscillators are usually employed to cover the requisite frequency range. Up to about 200 MHz, the FET oscillator shown in **fig. 7** has been proved successful.

Tests have shown that the specified Neosid inductor should be used in the interests of stability. With CV201, the tuning range of the oscillator, and thereby its tuning sensitivity, is made

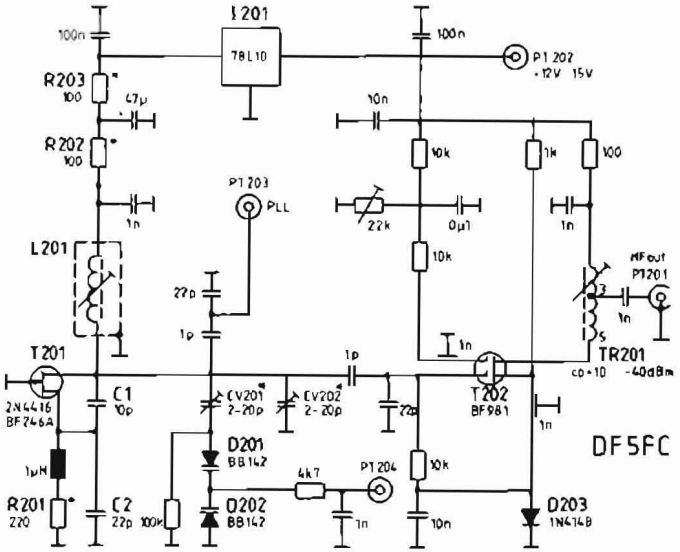


Fig. 7:
FET-Oscillator usable up to 200 MHz

adjustable. With CV202 and L201, the basic frequency range can be set.

After the oscillator, the signal is fed to a capacitive divider on the PLL buffer stage and then on to the oscillator amplifier. The oscillator amplifier has a dual-gate MOS-FET which allows a relatively large adjustment range of the output voltage and also possesses a high isolation to return signal energy. The power can be varied over a range from +10 dBm to −40 dBm.

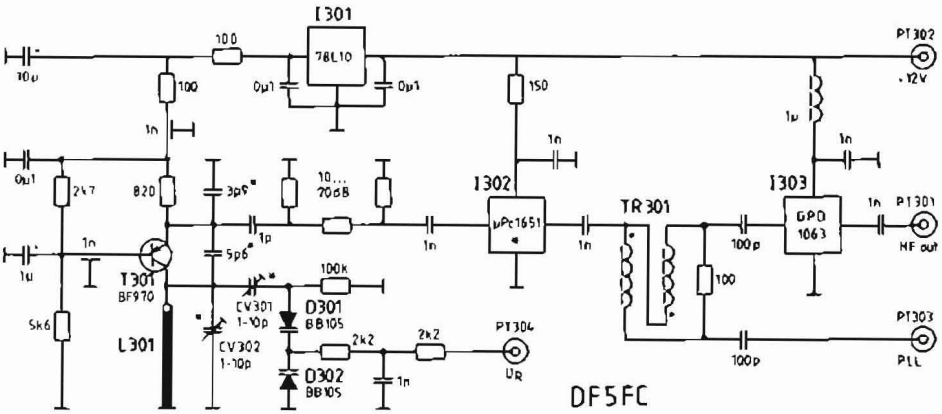


Fig. 8: Oscillator circuit for frequencies up to, or above 1 GHz (according to construction).
The tuned circuit can be realized from a length of semi-rigid cable, the length of which must be determined experimentally – start with 30 mm

The core of the output transformer can be any that is suitable for VHF, e g. Neosid or Siemens. Tests have confirmed that double-hole ferrite beads have proved themselves – they are used in the DJ7VY-amplifier, as well as the usual ring cores. The number of turns may remain unchanged between 50 MHz and 200 MHz.

### 3.3. Bi-Polar Oscillator up to ca. 1300 MHz

In the frequency range above 200 MHz, a circuit with a PNP transistor has proved itself in many tests. The advantage of the circuit shown in **figure 8** is that the tuned-circuit inductor is grounded at one end. This obviates trouble with the parasitic series inductance inherent to decoupling capacitors which is prone to cause spurious oscillations. The whole circuit construction must be carried out in accordance with VHF practice. This means, in particular, that the base and the cold end of the emitter resistor must be fitted with multi-layer chip capacitors sunk into the board. Careless work can result in drop-outs in the tuning range or reversal spots in the progression of tuning. This leads to completely unpredictable behaviour of the PLL. The de-coupling capacitors must be located as close as possible to the transistor. The transistor should be one of the given types, especially when working at the upper frequency limit. In any case, the various connecting sequences must be adhered to.

A length of short-circuited, semi-rigid coaxial cable is normally used with this type of oscillator which then functions as a capacitive shorted $\lambda/4$-wave tuned circuit. As both the inner and outer conductors of the line are bound rigidly together by the dielectric, the oscillator possesses excellent mechanical stability and shows little sign of microphony effects. The cable (e.g. Suhner type SR3), can be of either 50 Ω or 75 Ω characteristic impedance. The circuit can also operate either with a Lecher line or with a wound-inductor tuned circuit. The values given are dimensioned for a 70 cm equipment using a 21.4 MHz IF with the send frequency being produced directly. For other frequencies, the capacitors around the oscillator transistor, together with the varicap diodes' coupling capacitor, must be altered accordingly. Trimmer CV301 controls the frequency coverage of the oscillator and CV302 the basic frequency.

The buffer stage, in this case, comprises a 10 dB to 20 dB attenuator pad and an IC wideband amplifier, the NEC $\mu$PC1651. The circuit is designed so that there is at least 1 mW to 2 mW at the output of the amplifier.

Of course, other types of oscillators can be used here, among them the wide-range oscillators published in (8) or the semi-rigid VCOs in (9). Also of utility are the ceramic-resonator oscillators described in (10).

## 4. PROGRAMMING THE NJ8820

### 4.1. The IC's Internal Construction

The internal block schematic of the IC is shown in **figure 9**. The NJ8820 contains an 11-bit reference counter, a 7-bit A-counter and a 10-bit M-counter whereby the maximum division factors are set. The A- and the M-counter together control the switchable dividers via a logic circuit. When programming the reference counter (this controls the step frequency), care must be taken that the variable counter is followed by a fixed divide-by-two scaler.

All counters are equipped with registers connected with each other in order that 4-bit words can be registered externally. All bits together represent a 28-bit long word. To this 28-bit word, four make-up bits are added to make a total of 32 bits. This is split-up into eight 4-bit words which address the IC, via appropriate address logic, with a 3-bit wide address bus. The correct order of these bits is, of course, important for the correct control. The signal-timing schematic of **figure 10** shows the exact arrangement. The individual dividers will be treated with examples. The 00 stands for the make-up bits.

### 4.2. Deriving the Division Factors

#### 4.2.1. Reference Counter

The internal oscillator circuit is able to work with crystals of over 10 MHz. In order to determine

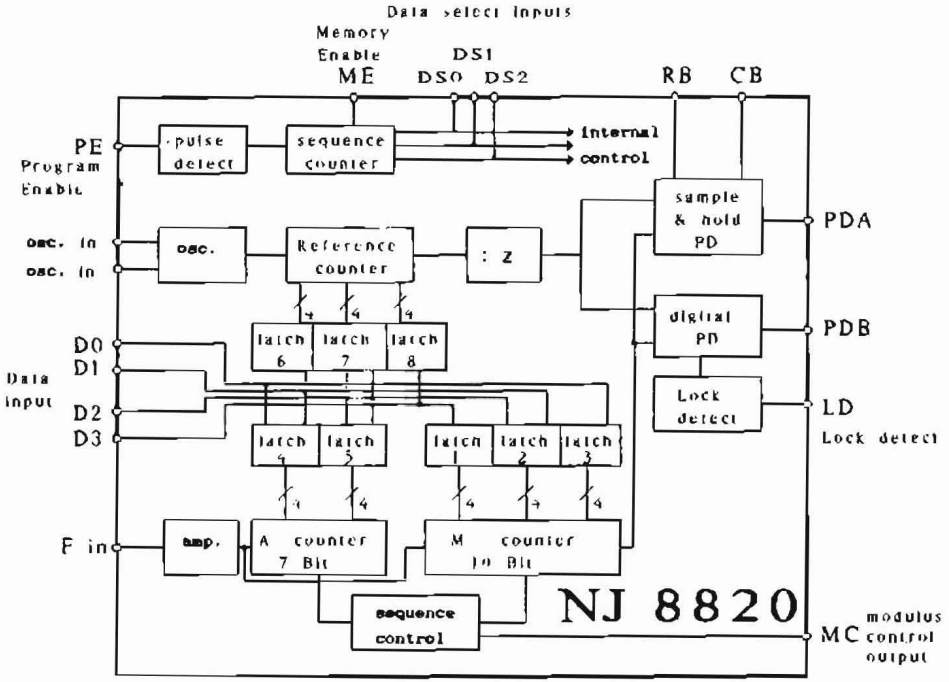


**Fig. 9: Interior of the PLL-chip module. It contains all the required dividers and control circuits**

the required division factor, the crystal frequency must be halved (internal : 2) and then divided by the reference frequency. The result must be a whole number. The division factor must then be expressed as a binary word.

$$R = f_{quarz}/(2 * f_{step}) \qquad (5)$$

Example: $f_q$ = 4 MHz, $f_s$ = 10 kHz

R = 4 MHz/(2 * 10 kHz) = 200 ≙ &0C8
= 000/1100/1000
(sequence R10...R0) = 11 bit

### 4.2.2. The A- and M-Control Counters

From the ratio of output frequency to reference frequency, the total division factor N is determined. For an N divider with a switchable prescaler the following expression applies:

$$N = f_{out}/f_{step} = (P * M) + A \qquad (6)$$

If N is divided by P the result is not a whole number. The value before the comma is substituted for M, the value after the comma is multiplied by P and the result is then A. Each value for M and A are transformed again into binary words and put into the appropriate places in the table (see para. 1.4.).

Example:
$F_{VCO}$ = 430 MHz – 439,99 MHz
channel step = 10 kHz ($f_{step}$)

$N_{max}$ = 439,99 MHz/10 kHz = 43999
P = 80 (SP 8719)

M = N/P = 43999/80 = 549,9875
= 549 ≙ &225 = 10/0010/0101
(series M9...M0) = 10 bit

A = 0,9875 * 80 = 79 ≙ &4f = 100/1111
(series A6...A0) = 7 bit

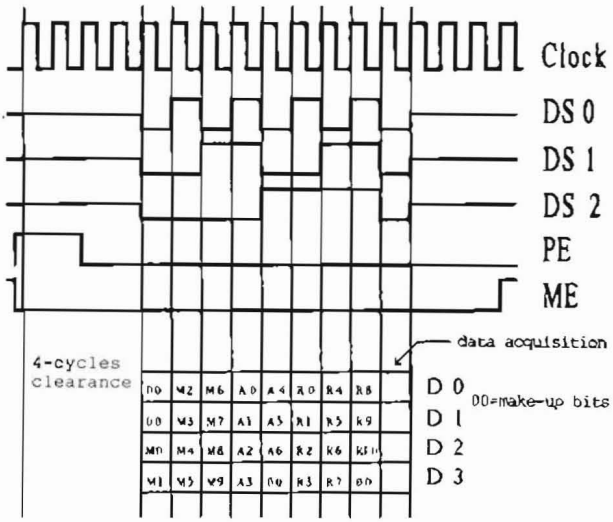


Fig. 10:
**Arrangement of the individual programming bits with respect to the PLL-ICs control signals**

### 4.3. Programming Units

The IC used here, retrieves the programming information automatically from the PROM or EPROM. In this manner, the PROMs for the receiver and transceiver are so programmed that in each case the transmit frequency is adjusted at the BCD switches. The switch-over to "transmit" and to "relay" operation is accomplished by changing the top address bits. The PROMs used here are only half exploited (4-bit words, for full exploitation a multiplexer must be connected to the data line).

The programming algorithms for such PROMs would be going a little too far for an article such as this as a good knowledge of mathematics is required. Ready-made PROMs for some standard applications (2 m with 10.7 MHz IF, 70 cm with 10.7 MHz IF with and without LO multiplier, 70 cm with 21.4 MHz IF with and without multiplier, simple 23 cm FM transceiver with 35 MHz IF) are available and the range will be expanded.

For the testing of the actual synthesizer function, particularly if it has not been pre-programmed, the circuit of **figure 11** has been developed.

The control signals of the synthesizer IC are used for addressing a total of 32 circuits. It can be seen that there are two blocks each having 16 bit and connected together with another multiplexer. In the prototype construction, DIL switches were employed in bunches of eight. When using toggle switches, 28 are enough, of course, but the four make-up bits should not be forgotten irrespective of whether they are 1 or 0. At the switches, the binary words are set to those values arrived at from the dividers (note the correct order). If available, hexa-decimal coded switches can be used whereby the correct arrangement of the bits must be observed.

When using the setting-up programming circuit, the signal lines must not be taken via feed-through capacitors as the impulses would be distorted during dynamic addressing operations. It is recommended that for this case a DIL plug is constructed, which is compatible with the PROM socket, and connect this, using a short flat-band cable, to the programming device.

At this juncture, a very important feature of the IC must be considered. All the transmitted bits are internally registered so that every 32-bit word is only needed to be sent once. The IC has an input (pin 14) at which can be switched to a permanent state of either address or read-in. If this input is returned to ground, the memory is permanently

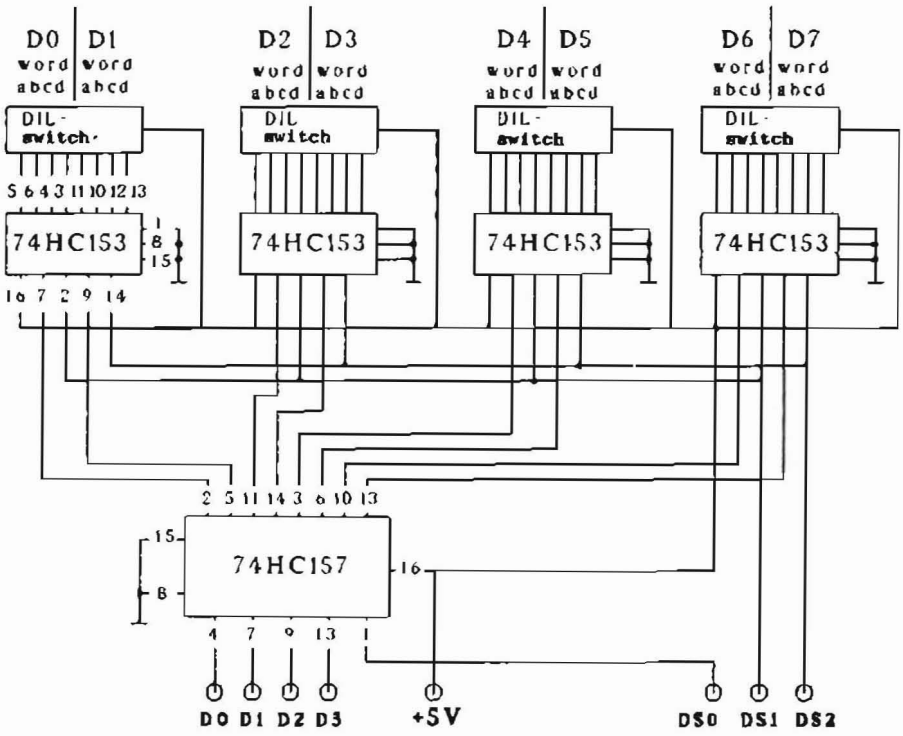


**Fig. 11: Auxiliary programming unit for the PLL-IC (only required if working without the E-PROM is required, e.g. for tests etc.)**

read out. It is also possible to apply a pulse at this input (either positive or negative) simultaneously with the arrival of the fresh input data.

Many circuits spring to mind for this sort of purpose. In the proposed synthesizer circuit, the lowest value bit is assessed from every BCD switch. As this is changed from 1 to 0 (or vice versa), the polarity across the capacitor also changes and its charge/discharge energy can be used as an impulse. Unfortunately, it turned out that the type of BCD switch chosen, operated too slowly. The resulting pulse, therefore is a little truncated and the IC does not respond. To improve this, a CMOS Schmitt trigger IC, type 74HC(T)14 was provided. The capacitor for the differentiation is located right behind this circuit. Before the gate inputs, there are integrators with a charge time of $\tau \approx 200$ ms in order to eliminate contact bounce in the BCD switches. This value seemed to be satisfactory for all types tried. If, however, there are some difficulties (false locks), the value can be increased to 1 s. Such a long time could cause problems on transmit/receive switch-over. The only real remedy is to try a better type of switch!

After these measures, no more difficulties were experienced. Of course, any type of Schmitt trigger-IC could have been tried in this position. When the synthesizer is in operation with the auxiliary programmer, the IC should be switched to either permanent interrogation or an additional push-button switch must be fitted.

A further important feature is the lock detector "LD". It lies at ground potential when the loop is in lock. For the control of external modules, it is taken out of the module. At PT 29, the original signal is available having an internal resistance of 1 kΩ, at PT 28, an open-collector output is available in order to drive an LED – as a simple application. Under transmit conditions, the transmitter should be suppressed by one of these outputs when frequency changes are being undertaken in order to avoid unwanted transmitter outputs.

## 5. CONSTRUCTION AND ALIGNMENT

Printed circuit boards have been developed for the actual synthesizer as well as for both oscillators. All three PCBs are double-foil, 1.5 mm thick epoxide-resin (imperative for HF). At least the synthesizer board should be provided with through-contacting as the component count is very high in some parts of the board. Experience has proved the value of using these professional practices in order to obviate the frustration caused by tracing grounding problems – such trouble quickly exceeds the extra expense.

The synthesizer board (layout plan in **fig. 12**) is of 70 cm x 70 cm dimensions and fits a standard tin-plate box. This type of construction is sufficient for the stability requirements of normal oscillators. The dimensions of both oscillator boards are identical at 70 cm x 35 cm (**figs. 13 and 14**), also fitting proprietary standard boxes. Furthermore, it is possible to solder them, complete with PCBs, into a yet larger enclosure.

All the DC-supply potentials are fed into the enclosures via feed-through capacitors. This also

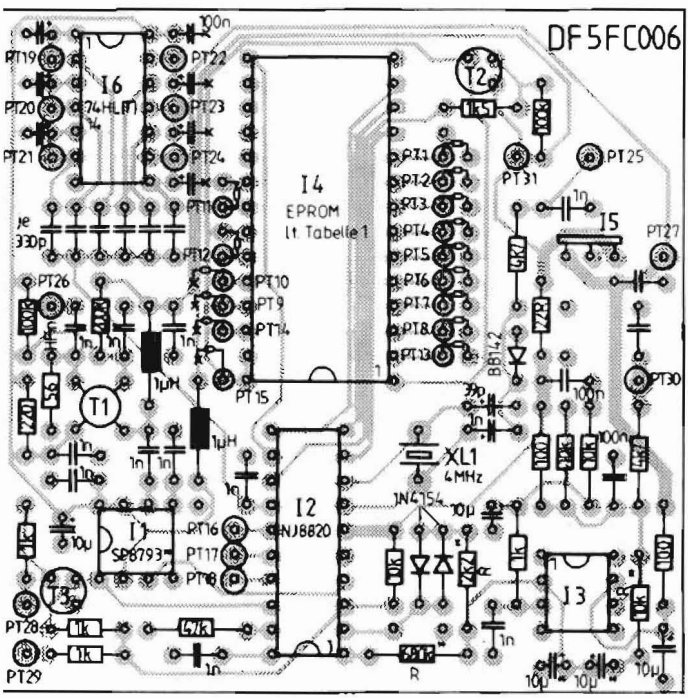


**Fig. 12:**
**Synthesizer PCB component layout plan**

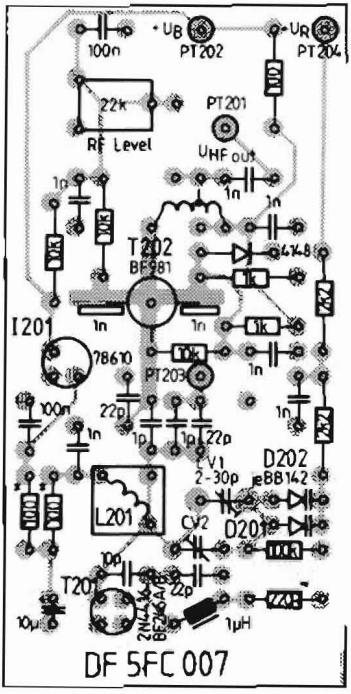


Fig. 13: FET-oscillator PCB component layout plan

applies to the loop control line. The RF connections use miniature coax connectors such as the well proven SMB or SMC series. Of course, the RF connection can just as well be soldered directly without using any connectors. The use of PTFE coaxial cable is recommended but this is more a question of price and availability.

Now for the actual construction. The synthesizer contains no internal adjustment possibilities! It has proved convenient to first of all solder the PCB into the pre-drilled housing and then load it later with components. This reduces the risk of a hot death for some components! The pre-scaler is soldered directly into the board but the other ICs can use sockets. Where the boards have not been designed to have circuit tracks on both sides, the removal of foil from around the non-grounded component pins should not be forgotten.

The board has been so designed, that the programme input pull-down resistors are soldered in an upright position. In this procedure, the resistor body is bent towards the groundplane. The free end is then taken to the feed-through capacitor (**see fig. 15**).

In this manner, many solder points and space is saved. Similar treatment is accorded to the Schmitt-trigger input resistors. They are connected by only one leg to the PCB, the second being connected directly with the appropriate

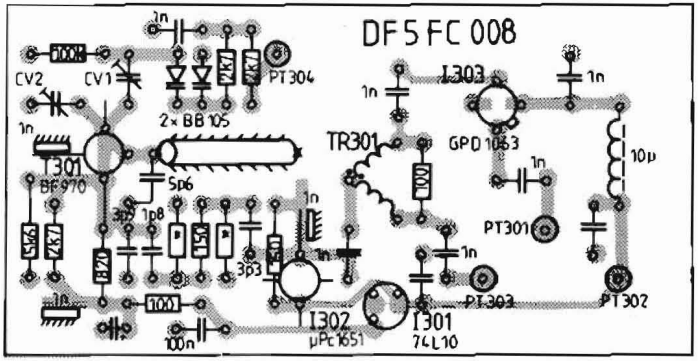


Fig. 14: GHz-oscillator PCB component layout plan. The resistors marked • belong to the attenuator pad and should only be equipped if required. Try semi-rigid cable 3 mm dia. Experiment with length!

feed-throughs. Furthermore, the EPROM address lines are taken through the board but directly to solder points so that they can be wired according to the type of PROM employed and the desired function of the sampling bits. It is important that the three bits that arrive via the switch, are connected to DS0, DS1 and DS2. The next bit is for the TX/RX switching, and the highest bit for the relay switching. This hierarchy is crucial for correct functioning and the "standard applications" are made clear in **table 1**.

The PCB for each oscillator should also be installed into the housing before loading with components. The construction of the oscillators must be carried out using great care. The drain voltages and currents of the FET oscillators are adjusted after installation. The best of adjusting them is to short out the drain resistor completely and change the source resistor until a current of 6 to 8 mA is obtained. Then, the source voltage is measured. To this value, 6 V are added as FET drain/source voltage and the total value of the matching drain is given by:

$$R_D = \frac{10\,V - (U_D + 6\,V)}{I_D} \qquad (7)$$

The resistor before the tantalum decoupling capacitor should always be more than 30 Ω. Since the FET, in the DC range, should always simulate a constant-current generator this procedure is permissable. The oscillator itself, has a very good phase-noise characteristic and lends itself well to other projects – in which case it may be worthwhile to employ high-grade voltage regulators (REF01 etc.)

The bipolar oscillators should oscillate immediately assuming that the components have been correctly installed. The PCB has been designed around the BF970 as the oscillator transistor. With other transistor types, the lead pin-outs must be observed.

The RF alignment is identical for the two types of oscillator. The trimmer CV01 determines the coupling of the varicap diodes and the CV02 the basic frequency. For the basic tuning, 5.5 V are applied to the voltage regulator input and CV01 is turned half-way.

### 5.1. FET Oscillator

The mid-frequency of the desired range is adjusted by L 201 with CV02 at about a third of its capacity. Trimmers CV201 and CV202 must now be iterated in order to achieve a tuning voltage range from 1 V to 11 V of the required frequency range plus an allowance of at least 1 MHz overlap. Taking a 2 metre application, this would mean a range of 132 MHz to 147 MHz. If the tuning range is not sufficient CV202 must be made smaller, CV201 must be enlarged and the alignment repeated. Altogether, the tuning range should be trimmed to be only as large as is necessary in order that the tuning sensitivity of the oscillator is not too great.

### 5.2. Bi-Polar Oscillator

The bi-polar oscillator has only two trimmers to align so that for the basic frequency adjustment, only CV302 is available. Both trimmers, again, must be iterated in order that the required tuning range is covered. This being for a 70 cm equipment 402 MHz to 442 MHz.

The PLL-filter calculations in the appendix are valid for these VCO sensitivities.

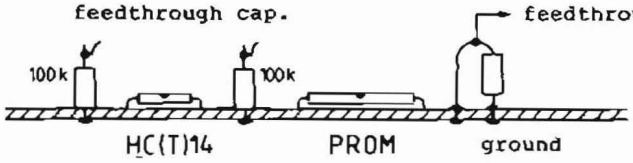


**Fig. 15: Constructional details for the connection of the program selector switch to the E-PROM and the impulse generator**

| A / PT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | DSØ | DS1 | DS2 | Schmitt-trigger-inputs | | | | | | min Eprom-type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPTION | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
| 1.) + 2.) | SØB | SØC | S1A | S1B | S1C | S1D | S2A | PT16 | PT17 | PT18 | Rx /Tx | relay | – | – | – | PT8 | PT9 | PT10 | PT1 | PT3 | PT7 | PT11 | PT12 | – | 27 64 27C64 |
| 3.) + 4.) | SØA | SØB | SØC | SØD | S1A | S1B | S1C | S1D | S2A | PT16 | PT17 | PT18 | Rx /Tx | relay | – | PT10 | PT11 | PT12 | PT1 | PT5 | PT9 | PT13 | PT14 | – | 27 128 27C128 |
| 5.) + 6.) + 7.) + 8.) | SØB | SØC | S1A | S1B | S1C | S1D | S2A | S1B | S2C | S2D | PT16 | PT17 | PT18 | Rx /Tx | relay | PT11 | PT12 | PT13 | PT1 | PT3 | PT7 | PT14 | PT15 | – | 27 256 27C256 |
| 9.) | SØA | SØB | SØC | SØD | S1A | S1B | S1C | S1D | S2A | PT16 | PT17 | PT18 | – | – | – | PT10 | PT11 | PT12 | PT1 | PT5 | PT9 | – | – | – | 27 64 27C64 |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | |

**Table 1: Connections of the synthesizer for the individual frequency ranges and E-PROMS. PT x in the second row from the top must always be connected with the corresponding point PT y in that column.**

**Arrangement of the BCD switches:**

| | |
|---|---|
| "Decade steps" | SØ - SØA...SØD |
| "Hundred kHz" | S1 - S1A...S1D |
| "MHz" | S2 - S2A...S2D |

**Option: reference crystal 4 MHz, pre-scaler factor P = 40**

1.) 2 m, 10.7 MHz IF, 25 kHz steps, LO multiplying factor = 1

2.) as 1, but multiplying factor = 3

3.) 2 m, 10.7 MHz IF, 10 kHz steps, multiplying factor = 1

4.) as 3, but multiplying factor = 3

5.) 70 cm, 10.7 MHz IF, 25 kHz, multiplying factor = 1

6.) as 5, but multiplying factor = 3

7.) as 5, but 21.4 MHz IF

8.) as 7, but multiplying factor = 3

9.) 136 - 138 MHz, IF = 10.7 MHz, 10 kHz steps, multiplying factor = 1

When this function is fulfilled, the PLL is considered as checked. A mid-frequency is selected and the PLL loop closed. With a correct functioning a mid-voltage will be measured and the correct frequency indicated on the counter. Also the "lock" LED must be extinguished. Check now (with an oscilloscope) the control voltage range by selecting various frequencies in the band. There must always be a DC voltage present for each selection. An alternating voltage component indicates an out of lock condition. If necessary, the tuning range can be trimmed with CV301 and CV302.

As can be seen from the circuit diagram, the reference crystal can be pulled on frequency by a varicap diode. In this manner, it is possible to realise a quasi-continuous tuning range. Some crystals are not able to be pulled to their nominal frequency. This is due to the deficit of coupling via the diode. In order to be able to achieve continuous operation, the PROM must be manufactured such that a frequency is always generated which lies one or two channels lower than the one displayed. If necessary, a little experimentation will have to be undertaken

## 6. PARTS LIST

### 6.1. Synthesizer Board

I1: SP 8792/A –: 80/81 up to 200 MHz
SP 8793/A –: 40/41 up to 200 MHz
SP 8716 –: 40/41 up to 520 MHz
SP 8718 –: 64/65 up to 520 MHz
SP 8719 –: 80/81 up to 520 MHz
according to frequency range

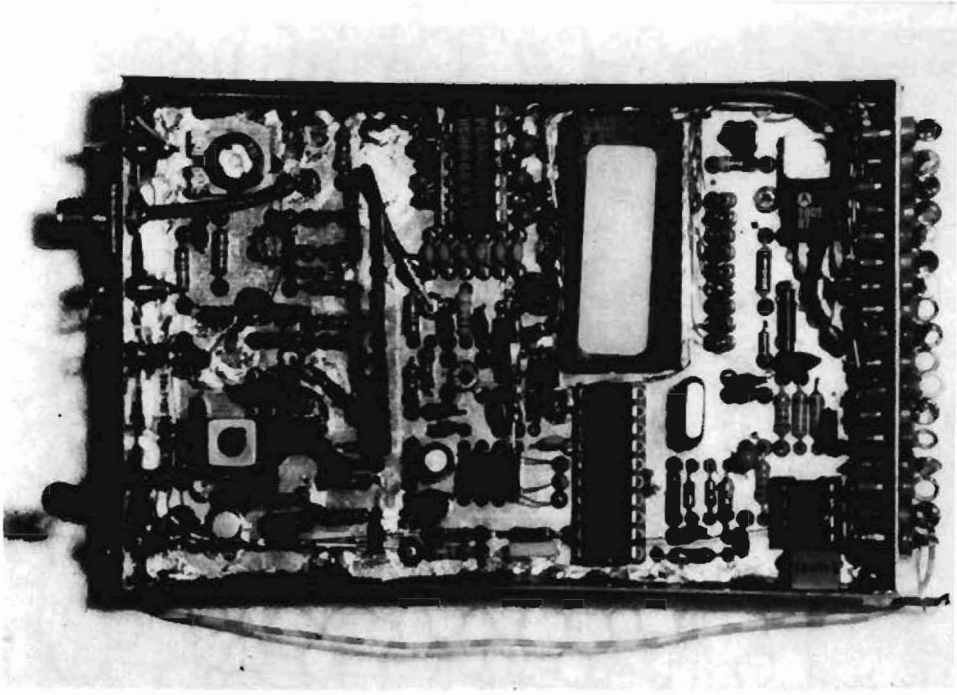

**Fig. 15: Sample construction according to figs. 12/13**

I2: NJ 8820
I3: NE 5534 or equiv. **low-noise** type!
I4: EPROM according to Table 1
I5: 7805
I6. 74HC(T)14

T1: BF 900/981 or equiv. up to 200 MHz
BF 966/988 or equiv. up to 1000 MHz
T2: BC 557 **B** (!) or equiv.
T3: BC 547 **B** (!) or equiv.

All capacitors have a 5.08 mm lead spacing and the resistors should suit a 7.62 mm grid.

$\mu$T means Tant. capacitors.
C2 should be a good quality foil type.
The values of R1, R2, R3 and C1/C1' depend upon the results of the loop-filter calculation.

### 6.2. FET-Oscillator

T201: 2N4416 or BF246A or B
T202: BF 900/981/963 or equiv.

I201: 78L10 (Ref 01, not adjusted for this project)

CV201: 2...40 pF
CV202: 2. .20 pF – try a fixed value 8.2 pF

R201:
R202:
R203:
} adjustment i.a.w. text – values given as a guide

TR201: 8-turns with tap at 3-turns on VHF core

D201/202: BB 142, BB 809

### 6.3. Bi-polar Oscillator

T301: BF 970 up to ca. 700 MHz
BFQ 23
BFQ 32
} up to 1300 MHz but different pin-out!

I 301: 78L10
I 302: Wideband amplifier e.g. NEC $\mu$PC1651 MAR-4 (Industrial Electronics)
I 303: Wideband amplifier GPD 1063 (AVANTEK)

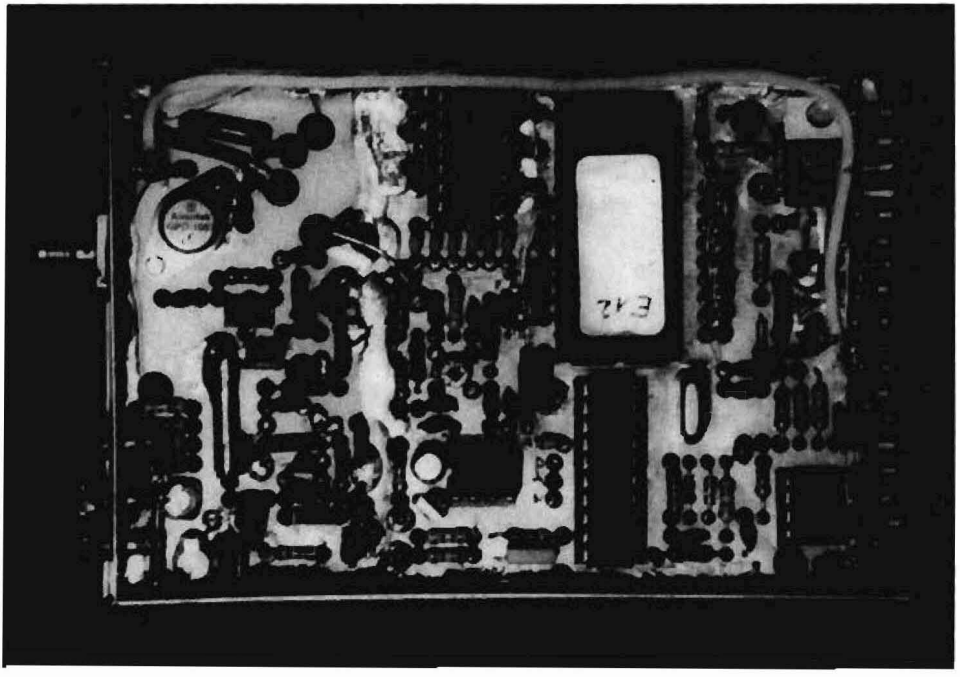

**Fig. 17: Sample construction according to figs. 12/14**

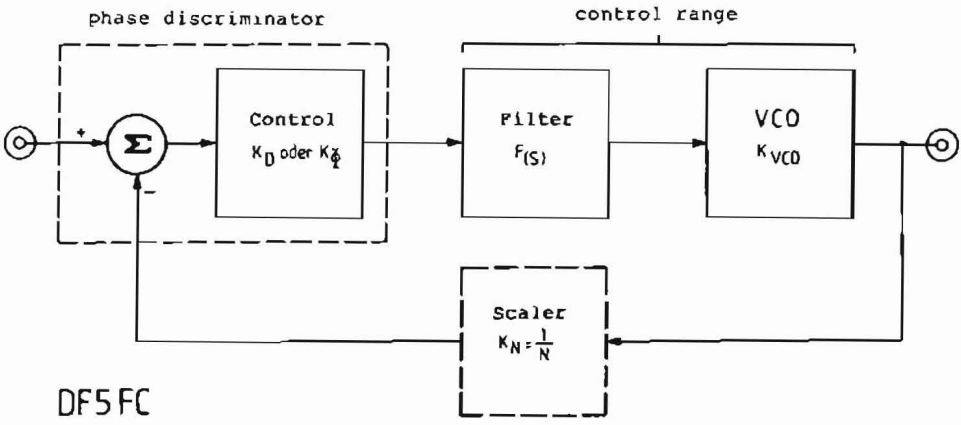


**Fig. 18: Basic circuit of a PLL-loop with the individual frequency dispositions**

TR 301: 2 x 4 turns on UHF core e.g. Siemens double-hole core
D 301 - 302: BB105

## 7. SUMMARY

**Pictures 16 and 17** show the author's specimen construction. This is a universal and versatile synthesizer circuit which is able to be integrated into many oscillator projects and can also be retro-fitted into other equipments. An enhancement of the control, using a $\mu$P together with the appropriate software, opens up other possibilities (e.g. signal generators), which until now have only been available in commercial test equipment.

## 8. APPENDIX LOOP FILTER – BASIC CALCULATIONS

A Phase-Locked-Loop (PLL) is a control structure in which a portion of the output signal is compared against a reference signal and from the result a correction factor for the output signal is derived (**fig. 18**).

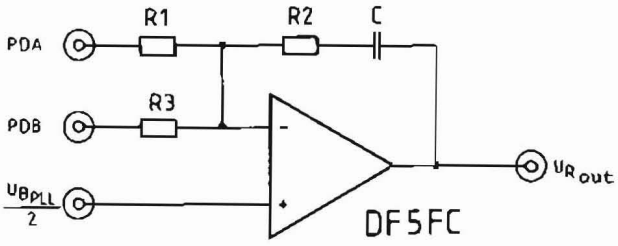


**Fig. 19: Basic circuit of an active loop-filter**

The behaviour of this loop, when input quantities are varied, is determined by quite a number of parameters. Many of these parameters are determined by the type of circuits selected for the oscillator, the phase detector and the divider. The only possibility in order to influence the behaviour of the loop, without going to a great deal of trouble, is to alter the loop filter. This filter can be either active, using an operational amplifier, or a passive RC network. The basic mathematics are thoroughly treated in (11). This describes the conditions suitable for the type of filter employed. The circuit under consideration here, uses an active filter employing a relatively low-noise OP. The basic circuit is shown in **fig. 19.**

The resistors R1 and R2 together with the capacitor C represent the universally known filter in the reference. The supplementary resistor R3, is employed for the double phase-detector. Such a filter offers the possibility of adjusting the so-called loop circuit-frequency ... and the attenuation D independently from one-another. With these quantities, the oscillatory conditions can be determined e.g. following a frequency change. If the circuit loop frequency is too low, the search time for the newly selected frequency will be high: when the attenuation is too small, it can occur that the loop doesn't lock in. The attenuation should amount to an aperiodic limit of between 0.7 and 1. The loop frequency can be very well approximated by the following expression:–

$$\omega_n = 2 * \pi * f_n \tag{8}$$

$$f_n = \frac{f_{ref}/100}{\sqrt{1 + 2 * D^2 + \sqrt{(1 + 2 * D^2)^2 + 1}}} = \frac{f_{ref}/100}{2{,}48} \text{ for } D = 1 \tag{9}$$

from this follows the dimensioning equation

$$\omega_n = 2 * \pi * f_{ref}/248 \tag{10}$$

Both these quantities allow the component values for the PLL to be arrived at.

$$\omega_n = \sqrt{\frac{K\Phi * K_{VCO}}{N * \tau_1}} \tag{11}$$

$$\tau_1 = R_1 * C \tag{12}$$

$$D = \frac{\tau_2}{2} * \omega_n \tag{13}$$

$$\tau_2 = R_2 * C \tag{14}$$

These four equations are generally applicable for any kind of PLL loop. The quantity $K_\Phi$ is the sensitivity of the phase-detector i.e. its output voltage per degree of phase difference between the input signals. The oscillator sensitivity is given by $K_{VCO}$ and is defined as the frequency alteration in Herz per volt of loop voltage change times $2\pi$.

In the circuit under discussion, the actual task of control is left to the analogue PD (A). When the circuit has achieved lock, it carries out the fine tuning control. Owing to the peculiarities of the design, the circuit noise is very well suppressed. A series of component formulas is now given:

$$C * R_2 = \frac{K_a * K_{VCO}}{\omega_n^2 * N} \tag{15}$$

$$R_1 \geq \frac{5 * R_2}{K_a} * \left( \frac{2 * D}{\omega_n} + 1 \right) \tag{16}$$

$$\frac{R_2}{R_3} = \frac{K_a * K_{VCO}}{2 * D * \omega_n * N} \tag{17}$$

$$K_{VCO} = \frac{\Delta f}{\Delta U} * 2 * \pi \tag{18}$$

where,

$f_n$ = working frequency of loop
$\omega_n$ = loop BW frequency
$K_a$ = PD (analogue) sensitivity
$K_d$ = PD (digital) sensitivity
$K_{VCO}$ = VCO tuning sensitivity ($2 * \pi$ * Hz/V)
D = attenuation normally unit but optionally 0.7
N = total division factor

According to the Plessey data-book (5), the sensitivity of other analogue PDs can be extracted from the circuit data as follows:–

$$K_a = 10 * \frac{U_B - 0{,}7 - 89/\sqrt{R_b}}{2 * \pi * 50 * 10^{-12} * R_b * f_r} \qquad (19)$$

where,
$R_b$ = the external resistor at pin 2
$f_r$ = step frequency (10 kHz in example)
$U_B$ = PLL-IC supply voltage

He who wishes to experiment further, will find all the necessary information in the references given.

Following this basic discussion, the calculation of all the important quantities specifically for the two important frequency bands, 2 metres and 70 cm will be carried out.

### 8.1. 2 m Synthesizer with a 10.7 MHz IF

VCO range for the transmitter:
144 MHz - 145.990 MHz
VCO range for the receiver:
133.3 MHz - 135.3 MHz
The total tuning range should have a minimum of 133.3 MHz to 145.99 MHz i.e. overlapping the required range by at least 1 MHz. From this results a $\Delta f$ of 15 MHz. The range of the tuning voltage should be from +1 V to +10 V (supply voltage minus the OP limits), $\Delta U$ is therefore 9 V. The average sensitivity of the oscillator, as given by formula (18), is:–

$$K_{VCO} = 2 * (5/3) * \pi * 10^6 \quad \text{rad/Vs}$$

From (19), the sensitivity $K_a = 300$ of the phase detector A can be determined. The reference frequency, i.e. the step frequency, should amount to 10 kHz. From formulae (8) to (10) $\omega_n$ to 250 1/s is obtained, whereby the actual value is rounded off from (253.35 1/s). The maximum division factor, from (3), is $N_{max} = 14599$, with this value, the worst case must be dimensioned. All the limit values have now been enumerated and the filter can now be calculated:

From (15) is obtained $C * R_2 = 3.56$ and from (17) $R_2/R_3 = 445.6$. With the result from (17), $R_2$ can now be determined. It should not be above 1 MΩ as the input resistance of the operational amplifier cannot be neglected. As a good compromise, the value of 910 kΩ can be taken (standard value), whereby $R_3$ has a value of 2.042 kΩ. For the time being, the larger standard value of (2.2 kΩ) should be employed. With (16), the minimum value of $R_1$ can be calculated. This should be larger than, or equal to 18.345 kΩ, this means a standard value of 22 kΩ. Finally, the result of (15) and the determination of $R_2$, the integration capacitor $C = 3.9\ \mu F$ can be calculated (4.7 $\mu$F used).

All the component values have now been evaluated and the loop should function optimally. Unfortunately, there are component tolerances that must be taken into consideration and the fact that all calculations based upon an OP have assumed that it is an ideal amplifier. This means

Table 2

| | | |
|---|---|---|
| $N_{min\ Tx}$ = 14400 | M = 360 ≙ 01/0110/1000 | A = 0 ≙ 000/0000 |
| $N_{max\ Tx}$ = 14599 | M = 364 ≙ 01/0110/1100 | A = 39 ≙ 010/0111 |
| $N_{min\ Rx}$ = 13330 | M = 333 ≙ 01/0100/1101 | A = 10 ≙ 000/1010 |
| $N_{max\ Rx}$ = 13529 | M = 338 ≙ 01/0101/0010 | A = 9 ≙ 000/1001 |

Table 3

| | | |
|---|---|---|
| $N_{min\ Tx}$ = 17200 | M = 215 ≙ 00/1101/0111 | A = 0 ≙ 000/0000 |
| $N_{max\ Tx}$ = 17599 | M = 219 ≙ 00/1101/1011 | A = 79 ≙ 100/1111 |
| $N_{min\ Rx}$ 16344 | M = 204 ≙ 00/1100/1100 | A = 24 ≙ 001/1000 |
| $N_{max\ Rx}$ = 16743 | M = 209 ≙ 00/1101/0001 | A = 23 ≙ 001/0111 |
| Series | M9...M0 | A6 ..A0 |

that an inspection of the output signal with a spectrum analyzer, or a receiver, and possibly some cut and try work may be necessary. Individual cases may call for some experimentation, as there can be no general recipe for an optimal solution.

The reference oscillator is equipped with a 4 MHz crystal. According to formula (5), the reference divider must be adjusted to the value R = 200. Expressed as a binary word, this amounts to: R = 200 (binary): 000/1100/1000 in the series R10...R0.

The divider factors for the programming device are determined according to the expressions (3), (4) and (6). Their respective binary values are appended. Only the limit frequencies have been calculated (P = 40) (**table 2**).

### 8.2. 70 cm Synthesizer with a 21.4 MHz IF

Send frequency: 430 MHz - 439.975 MHz
Receive frequency: 430 MHz - 418.575 MHz
Frequency span: $\Delta f = 36$ MHz
Tuning voltage range: $\Delta U = 9$ V
Oscillator sensitivity (from 18): $K_{VCO} = 2 * \pi * 10^6$ rad/Vs
Phase-detector sensitivity (19): $K_a = 300$
Loop frequency (10): $\omega_n = 600$ 1/s
Reference (step) frequency: $f_{ref} = 25$ kHz
maximal division factor from (3): $N_{max} = 17599$

Hence:
from (15): $C * R_2 = 1.19$
from (17): $R_2/R_3 = 357$
$R_2$ rounded to 680 kΩ, $R_3$ to 2 kΩ
$R_1$ must equal or be greater than 12 kΩ, 15 kΩ used

C = determined from (15) and the value of $R_2$
1.75 µF, 2.2 µF used

Finally, the division factors for the programming device are given in **table 3**.

The reference oscillator also uses a 4 MHz crystal. From (5)

R = 80 ≙ 000/0101/0000 series R10...R0

## 9. LITERATURE


(1) Becker, J., DJ 8 IL: "SUEDWIND" 2 m FM hand-held Transceiver with 80 or 396 Channel Synthesizer and Touch-Key Operation.
Part 1: Circuit Description
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